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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00203788.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Titre de l'invention:
Supply circuit

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Supply circuit

The present invention relates to a circuit arrangement of transistors, particularly of JFETs, for use in supply circuits, particularly for high voltage integrated circuits (ICs).

According to the prior art such a circuit comprises a transistor connected between a high voltage supply and a load, e.g. a capacitor, and has its gate connected to ground to dissipate the multiplication current to ground. This leads to dissipation without any use.

It is an object of the invention to provide a supply circuit with a reduced dissipation and/or (multiplication) current loss. To this end, the invention provides a supply circuit as defined in the independent claims. Advantageous embodiments are defined in the dependent claims.

According to one aspect of the invention, there is provided a circuit comprising a first transistor, preferably a JFET, connected in series to a second transistor, also preferably a JFET, wherein the gate of the first transistor is connected to the source of the second transistor and is not connected to ground. The gate of the second transistor is preferably connected to ground.

Preferably the transistors are JFET transistors and at least the first JFET transistor is advantageously formed by a silicon on insulator (SOI) integration technology, for example as described in applicant's non-prepublished European application 99 204 404.0 (attorneys' docket PHN 17.807).

According to a preferred embodiment the first transistor is a high voltage JFET and the second transistor is a low voltage JFET. This circuit configuration is particularly advantageous when used to regulate the voltage to charge a capacitor and is applicable to lighting IC and power supply applications. The circuit is substantially multiplication independent.

The unique circuit configuration reduces the power loss through the ground connection of the gate of the second transistor because multiplication current from the gate of

the first transistor bypasses the second transistor and is fed directly into the current path of the source of the second transistor.

For a better understanding of the present invention and to show how it may be carried into effect, reference will now be made, by way of example, to the accompanying drawings.

In the drawings:

Fig. 1 is a circuit diagram of a prior art circuit;

Fig. 2 is a circuit diagram of a circuit according to the present invention; and

Fig. 3 is a cross-section through a JFET made by a silicon-on-insulator process that is suitable for use in the circuit of Fig. 2.

Fig. 1 shows a circuit for a junction isolated process with a JFET 12 connected between a high voltage supply 13 and a load comprising a capacitor 14 and current source 17. The gate 15 of the JFET 12 is connected to ground so as to sink the multiplication current 16 Imult of the JFET 12 to ground to reduce its contribution to the regulated voltage node.

Typically the high voltage supply 13 would supply 650 V and assuming a typical multiplication factor M=2 for the circuit of Fig. 1 then the multiplication current 16 Imult to ground will be 250 μA, and will be the same as the load current 17 load across the capacitor 14, for a typical regulated voltage of 40 V. Although the multiplication current 16 Imult does not contribute to the regulated voltage node, it does contribute to the power dissipation. In this example the total power dissipation is 0.33 W of which 0.16 W is due to the multiplication current 16 Imult being led to ground.

In Fig. 2 the circuit of the invention comprises two JFETs 21 and 22 connected in series between a high voltage power supply 23 and a load comprising a capacitor 24 and a current source 30. The capacitor 24 serves to flatten fluctuations at the load 30. While in this drawing, the load is represented by a current source 30, it may be any load that needs a regulated voltage. The circuit of Fig. 2 could be used as a start-up circuit in a high-voltage IC such as used in a switched mode power supply for televisions, in which case the load would be formed by other circuits in the high-voltage IC. It could be used in a lighting IC to switch on lighting equipment.

The gate 25 of the JFET 22 is connected to ground but the gate 26 of JFET 21 is connected to the source of JFET 22 at node 27 and is not connected to ground. The JFET

21, and advantageously also JFET 22, is preferably formed by a silicon-on-insulator process as described in EP 99 204 404.0.

In the example illustrated with a power supply 23 of maximally 650 V (but normally, absent from any power fluctuations, being around 240 $\sqrt{2}$ V), the multiplication current 28 Imult1 at the gate of JFET 21 is 125 μA and the load 29 current Iload1 through the JFET 21 is 125 μA. For a regulated voltage Vpinch typically of 40 V at the node 27, the load current 30 Iload2 across the capacitor 24 needs to be 250 μA and this comprises the sum of Iload1 (29) and Imult1 (28). No multiplication current from JFET 21 is thus lost. The multiplication current Imult2 from JFET 22 is small or non-existent because the drain voltage on JFET 22 is small. Thus in this example the power dissipation is reduced by 50%, compared to the circuit of Fig. 1, to 0.16 W.

Fig. 3 illustrates a typical silicon-on-insulator JFET transistor as described in EP 99 204 404.0. The circuit comprises a semiconductor body 303, in this example made of silicon, with a semiconductor layer 305 of a first conductivity type, of n-type silicon in this example of an n-channel transistor, adjoining the surface 304. The thickness and the doping concentration of the layer 305 are, for example, 1 to 1.5 μm and 10^{16} to 5×10^{16} atoms per cm^3. The silicon layer 305 is bounded at the side opposed to the surface 304 by a layer 306 of electrically insulating material which insulates the silicon layer 305 from the subjacent silicon substrate 307. The substrate 307 is preferably n-type doped. The layers 305 and 306 form a SOI (Silicon On Insulator) structure which may be manufactured in various ways which are known per se. Thus the layer 306 may be formed, for example, by a layer of aluminum oxide (sapphire) on which the silicon layer 305 is epitaxially grown. Other techniques which may advantageously be used are "smart cut" and "wafer bonding" techniques, whereby two crystals, of which at least one is provided with an oxide layer, are fastened to one another, whereupon the silicon layer 305 can be manufactured from one of the crystals through etching or polishing. In the present example, the insulating layer 306 is formed by a buried layer of silicon oxide which is obtained in a known manner by a smart cut technique. The thickness of the layer 306 is approximately 3 μm.

Islands which are mutually electrically insulated, for example by means of regions 308 of silicon oxide extending transversely across the thickness of the silicon layer 305, are formed in the layer 305. The transistor comprises a source in the form of a strongly doped n-type surface zone 309 and a drain in the form of a strongly doped surface zone 310. The source and the drain are connected to a metal contact 311 and a metal contact 312,

respectively. The drain lies around the source in this embodiment, but it will be obvious that alternative configurations are equally possible. A channel region 313 formed by a portion of the island-shaped n-type silicon layer 305 is situated between the source 309 and the drain 310. A gate 314 in the form of an n-type doped polycrystalline silicon layer, referred to as poly for short hereinafter, is provided above the channel region. The channel and the gate are separated from one another by a layer 315 of silicon oxide which forms the gate dielectric of the transistor. The thickness of the oxide layer 315 is approximately 0.8 μm in the present example of a high-voltage transistor. Some other suitable material may be chosen instead of silicon oxide for the gate dielectric.

The transistor forms a depletion MOS transistor in which a depletion region is induced in the channel by a negative voltage (with respect to the source) at the gate 314, which controls the conduction between source and drain. When the depletion region pinches the channel at a sufficiently high voltage at the drain, the transistor is in the pinch state. To prevent inversion occurring at the boundary between the channel 313 and the gate oxide 315 and at the boundary between the channel 313 and the buried oxide layer 306 in this state, the n-type silicon layer 305 is provided with at least one p-type zone 316 (having a higher doted contact zone) which forms a pn junction 317 with the channel and which extends transversely across the thickness of the channel 313. To obtain an efficient charge removal for any width of the channel, adapted to the specific application, a number of zones 316 distributed over the channel width are provided in the semiconductor layer. Most of these zones are rectangular in shape; the zones 316 at either end of the transistor have a curved shape and cover the entire bend in the channel. This, however, is not necessarily the case; it is alternatively possible for small zones 316 to be formed at the ends, mutually separated by portions of the channel. The shape of the zones 316 at either end as shown here has certain advantages for design technology which arise from the chosen oval shape of the transistor. In an embodiment in which the transistor is not oval but, for example, rectangular, it is obvious that mutually separated zones 316 may be used at the ends. To prevent the pinch voltage being determined by depletion caused by the zones 316 (as in a junction field effect transistor), the zones should be situated at sufficiently great distances from one another, as compared with the channel thickness. On the other hand, the zones 316 are preferably situated so closely together, for an efficient removal of minority charge carriers, that a small, laterally directed field is present across the entire width of the channel, such that holes drift towards the zones 316. In the present example with a channel thickness of 1 μm, a value of 15 μm was chosen

for the interspacings between the zones 316, which was found to be a favorable value which satisfies both conditions set out above.

The transistor is provided with a drift region 318 between the channel 313 and the drain 310 with a length of, for example, 70 μm in view of the high voltages that may be applied to the drain. The semiconductor layer 303 is provided with a thinned portion at the area of the drift region, in this example formed in that the layer 305 is oxidized through a greater portion of its thickness than at the area of the channel 313. The oxide layer 319 above the drift region 318 has a thickness of approximately 2.0 μm and is accordingly substantially thicker than the silicon oxide layer 315 which forms the gate dielectric of the transistor and which has a thickness of approximately 0.8 μm. A further silicon oxide layer 320, for example in the form of a deposited TEOS layer, is provided on the gate electrode 314 and the oxide layer 319, on which layer 320 a metal field plate 321 is provided. The function of such a field plate, which provides a higher breakdown voltage in combination with a low on-resistance through an improvement in the field distribution, is known. The field plate is connected to the gate 314 and to the p-type zones 316 through contact windows in the oxide layer 320. The gate voltage is accordingly applied to the field plate 320 and the p-type zones 316. Obviously, the zones 316 and/or the field plate may also be connected to other junction points in the circuit, such that other voltages are applied to these regions. The source and drain contacts 311 and 312 are also provided in the oxide layer 320 via contact windows. The field plate 321 may be formed at the same time as the metal contacts 311 and 312.

The thickness of the silicon oxide layer 320 is approximately 0.5 μm. The total thickness of the layers 319 and 320 is accordingly approximately 2.5 μm and is thus equal or at least substantially equal to the thickness of the buried oxide layer 306. Since equal or substantially equal voltages are applied to the gate electrode and the substrate 307 during operation, an electrically substantially symmetrical situation is obtained by means of the equal oxide thicknesses, which is favorable for the electric field distribution and thus for the breakdown voltage of the transistor. A further improvement may be obtained in that the drift region 318 is provided with a profiled doping whose concentration increases linearly in the direction from the source to the drain.

So, the JFET transistor preferably used in the present invention is a deep depletion MOS transistor provided in a thin silicon layer 305 adjoining a surface 304 of a silicon body 303 and isolated from a silicon substrate 307 by a buried oxide layer 306. The channel region 313 of a first conductivity type is provided with at least one and preferably a plurality of surface adjoining zones 316 of the opposite conductivity type to remove minority

carriers from the interface between the channel and the gate oxide 315. The zones 316 extend across the whole thickness of the channel region 313 and adjoin the buried oxide layer 306 at the side of the channel region 313 remote from the gate dielectric. Due to this construction, minority carriers are removed also from the rear side of the channel region 313. This enables the transistor to be operative also at high voltages having values at which the substrate 307 and the buried oxide layer 306 are operative respectively as a second gate an a second gate dielectric.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS:

1. A voltage supply circuit, comprising:

a first transistor (21) having a main electrode, and a control electrode that is not directly connected to ground; and

a second transistor (22) having a first main electrode coupled to the main electrode of the first transistor (21), and a second main electrode for supplying a regulated voltage, the second main electrode being coupled to the control electrode (26) of the first transistor (21).

2. A circuit according to claim 1 wherein the first transistor (21) is a JFET.

3. A circuit according to claim 2 wherein the second transistor (22) is a JFET.

4. A circuit according to claim 1, wherein a gate (25) of the second transistor (22) is connected to ground.

5. A circuit according to claim 1, wherein the first transistor (21) is formed by a silicon-on-insulator (SOI) integration technology.

6. A circuit according to claim 1, wherein the second transistor (22) is formed by a silicon-on-insulator (SOI) integration technology.

7. A circuit according to claim 1, wherein the first transistor (21) is a high voltage JFET and the second transistor (22) is a low voltage JFET.

8. A circuit according to claim 1, further comprising a load (24, 30) coupled to the second main electrode of the second transistor (22) to receive the regulated voltage.

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ABSTRACT:

A circuit comprises a first JFET (21) connected in series to a second JFET (22) wherein a gate (26) of the first JFET (21) is connected to a source of the second JFET (22) and is connected to a load (30) and is not connected to ground. The gate of the second JFET (22) is connected to ground. The JFETs are preferably formed by silicon on insulator integration technology.

(Fig. 2)

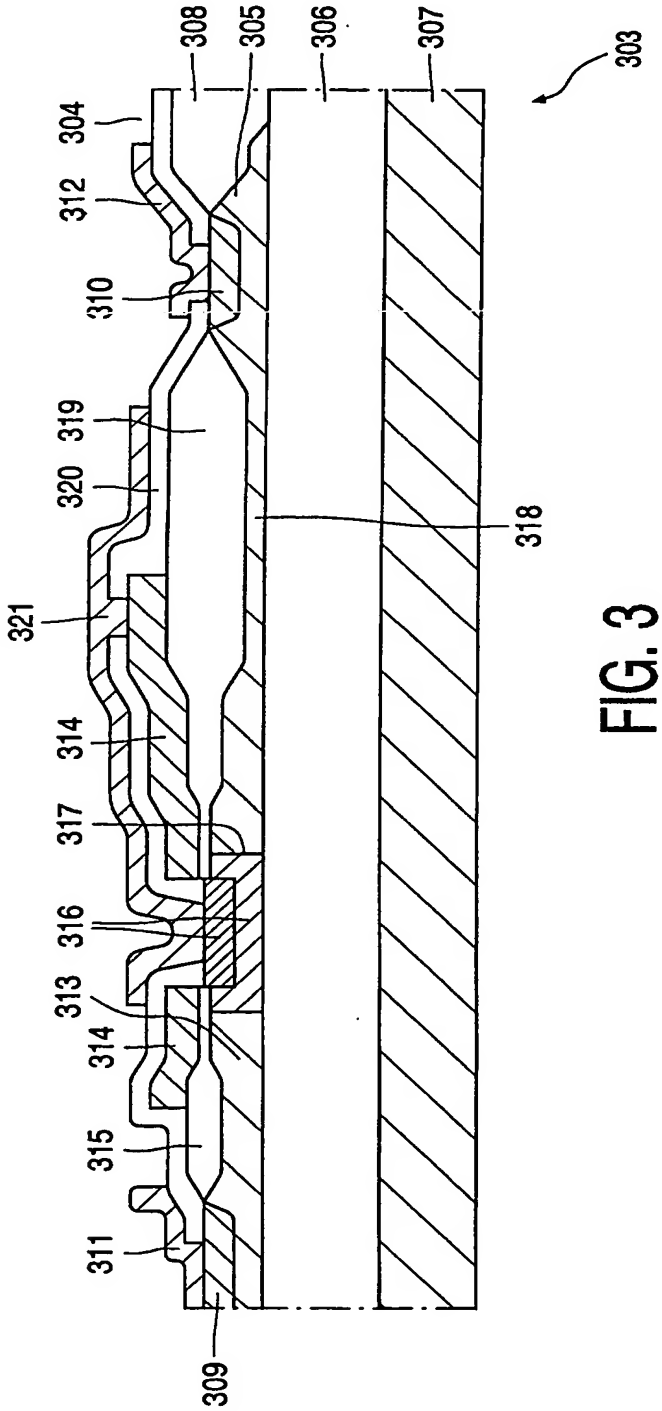
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FIG. 3

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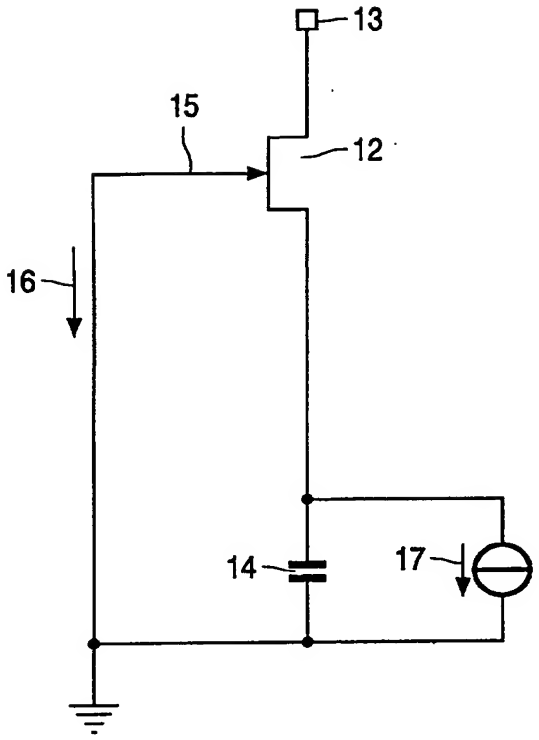

FIG. 1

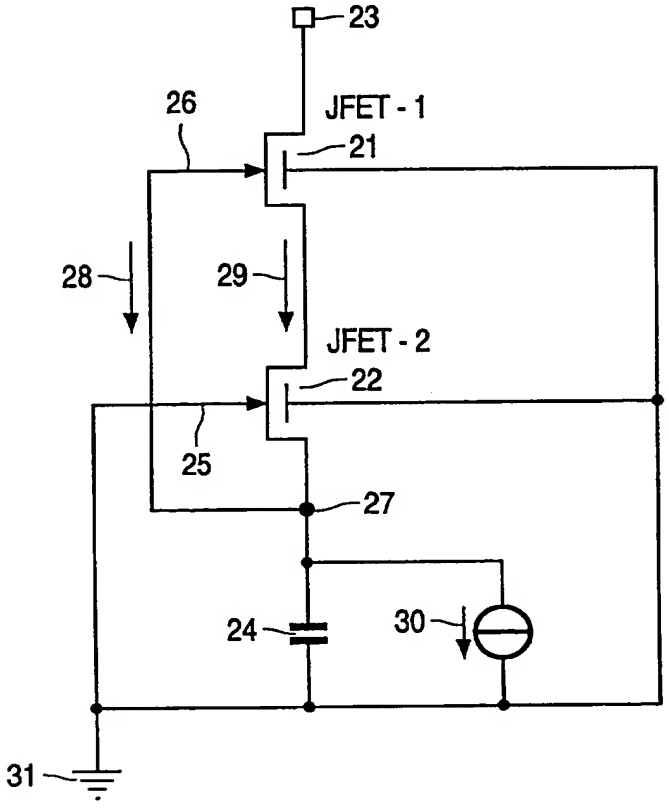

FIG. 2